Characterisation Of The NA62 GigaTracker End Of Column Readout ASIC

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TWEPP-10.
20\textsuperscript{th}-24\textsuperscript{th} September 2010
Aachen.

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1. GTK Architecture and Requirements

2. Demonstrator ASIC

3. Testing Ethos and Methodology

4. Results
   - TDC Performance
   - Test Pixel Performance
   - Electrical Charge Injection: ASIC Full Chain

5. Synopsis
1 GTK Architecture and Requirements

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5 Synopsis
The GigaTracker

- Mag1
- Mag2
- Mag3
- Mag4

- GTK1
- GTK2
- GTK3

- 60 mm
- 13.2 m
- 9.6 m
- 250 m

- $p_\pi$
- $p_k$
- $\theta_{\pi K}$
Beam Profile

60 mm

27 mm
GTK Architecture and Requirements

Beam and Detector Profile

- Width: 60 mm
- Height: 27 mm
- Height of the profile: 13.5 mm
- Height of the profile: 4.5-6 mm
- S.P13 rate: 1 MHz/mm², total rate: 1 GHz
## GigaTracker Requirements

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Radiation Environment</td>
<td>$10^{14} \text{n cm}^{-2} \text{yr}^{-1}$</td>
</tr>
<tr>
<td>Columns/Readout Chip</td>
<td>40</td>
</tr>
<tr>
<td>Pixels/Column</td>
<td>45</td>
</tr>
<tr>
<td>Pixel Size</td>
<td>$300 \mu m \times 300 \mu m$</td>
</tr>
<tr>
<td>Beam Rate</td>
<td>$800 \text{MHz} \rightarrow 1 \text{GHz}$</td>
</tr>
<tr>
<td>Dynamic Range</td>
<td>$\sim 1fC \rightarrow 10fC$</td>
</tr>
<tr>
<td>$Q_{MP}$</td>
<td>$2.4fC$</td>
</tr>
<tr>
<td>Front End Peaking Time</td>
<td>$\sim 4\text{ns}$</td>
</tr>
<tr>
<td>Time Binning</td>
<td>$\sim 97\text{ps}$</td>
</tr>
<tr>
<td>Momentum Resolution</td>
<td>0.4%</td>
</tr>
<tr>
<td>Efficiency</td>
<td>$\geq 99%$</td>
</tr>
</tbody>
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5. Synopsis
EoC Design Overview

Final ASIC: x 40

Single Test Column: 45 Pixels

On-Chip Transmission lines

Hit Arbiter

Hit Register 8

Hit Register 2

Hit Register 1

Hit Register 0

DLL

Coarse Counters

Pixel Array: x 1
x 20
x 40

End Of Column

Final ASIC: x 40

4 x 1.5Gbit/s
2 x 3 Gbit/s

End Of Column

Hit Register 0

Hit Register 1

Hit Register 2

Hit Register 8

Pixel 44
Pixel 43
Pixel 42
Pixel 0

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NA62 GTK EOC

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320 MHz clock, 32 starved delay cells → 97 ps time bin.
Time Over Threshold Time Walk Correction

- Pre-Amp Output
- Discriminator Output
- Peaking Time = 4 ns
- Time Walk
- Time Over Threshold

\( V_{\text{Threshold}} \)

\( T_0 \), \( T_1 \), \( T_2 \)
EoC: Chip Top Level Layout
EoC: Chip Top Level Layout

- **test pads**
- **test pixels**
- **1 folded column of 45 pixels**
- **EOC**
- **pads**
EoC Chip
EoC Assembly
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Mechanisms

- **Electrical**
  - 20 $fF$ Charge injection capacitor included in the pixel
  - Voltage step induces charge injection at front end of 1 (or more) pixel(s)
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  - Absolute gain calibration from pulse height spectra (analogue pixel)
  - $^{109}$Cd and $^{241}$Am $\gamma$ emissions used
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- **Laser Charge Injection**
  - 60 $ps$ FWHM, 1060 $nm$ Laser
  - Light pulse timing is good to $\sim 5 ps$ RMS
  - spot size $\sim 10 \mu m$ at focal distance
  - X-Y stage to scan laser spot across pixel matrix
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- **Beam test**
  - 10\( GeV \) \( \pi^+ / p^+ \) beam at PS (T9)
  - 4 cards placed in beam with GasTOF
  - underway now (16\(^{th}\) \( \rightarrow \) 29\(^{th}\) September 2010)
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TDC Performance
EoC TDC Non-Linearity

Differential:

Integral:

DLL TDC Jitter = 7 ps
Test Pixel Performance
T1 RMS Jitter: Qin and Qth

Electrical charge injection.
No detector
≈ 40 ps RMS at 2.4 fC
ENC ≈ 130 e⁻

Laser Charge Injection.
Detector biased at 300V.
≈ 70 ps RMS at 2.4 fC
ENC ≈ 180 e⁻
Analogue Pixel Pulse Height Spectrum with $^{241}\text{Am}$
T1 RMS Jitter: Operation Frequency

- **T1 RMS Jitter (s)**
- **Frequency (kHz)**
- **Qin=1.0fC**
- **Qin=1.2fC**
- **Qin=1.4fC**
- **Qin=1.6fC**
- **Qin=1.8fC**
- **Qin=2.0fC**
- **Qin=3.0fC**
- **Qin=4.0fC**
- **Qin=5.0fC**
- **Qin=6.0fC**
- **Qin=7.0fC**
- **Qin=8.0fC**
- **Qin=9.0fC**
- **Qin=10.0fC**

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Electrical Charge Injection: ASIC Full Chain
T0 Transfer Function

TDC Time vs Pulse Generator Offset, Qinj=3fC
T0 and T1 as a function of Injected Charge

Measured and Corrected times as a function of Q

Uncorrected
Corrected
RMS T0 Jitter Vs Q: Average Case

Mean T0 RMS Jitter

Time walk compensated, full chain readout, all pixels firing.
Systematic (uncorrectable) Residual TimeWalk

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5. Synopsis
The GigaTracker represents a very challenging project

- $< 200\,\text{ps}$ RMS time resolution
- $> 800\,\text{MHz}$ beam rate
- Harsh radiation environment
- $< 0.5\% X_0$
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Demonstrator ASIC and detector implemented
- DLL Based TDC which gives \(97\, ps\) nominal time binning
  - monotonic behaviour
  - RMS DNL \(\sim 0.17\, LSBs\)
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Excellent Pixel Performance
- Leading Edge Jitter $\sim$ 40 $ps$ bare ASIC at 2.4 $fC$
- Leading Edge Jitter $\sim$ 70 $ps$ Full depleted sensor with light injection at 2.4 $fC$
Synopsis

- The GigaTracker represents a very challenging project
  - < 200 $ps$ RMS time resolution
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- Excellent Pixel Performance
  - Leading Edge Jitter $\sim 40 \text{ ps}$ bare ASIC at 2.4 $fC$
  - Leading Edge Jitter $\sim 70 \text{ ps}$ Full depleted sensor with light injection at 2.4 $fC$
- Full chain and time walk correction
  - timewalk correction mechanism shown to work well
  - Residual systematic remainder < 15 $ps$ RMS
  - RMS T0 Jitter $\sim 70 \text{ ps}$ at 2.4 $fC$ (bare ASIC)
Backup Slides
Chips 6 Full Column S-Curve @ 50V

digital s-curve for pixel 1

Charges $1.0 \, fC \rightarrow 5.5 \, fC$
digital s-curve for pixel 1
Chip 6 Full Column Transfer Functions @ 50V

Peaking Height (mV)

All 45 pixels from the full column are shown here
Chip 6: Distribution of Pixel Gains

<table>
<thead>
<tr>
<th>pixel_gains</th>
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<tbody>
<tr>
<td>Entries</td>
</tr>
<tr>
<td>Mean</td>
</tr>
<tr>
<td>RMS</td>
</tr>
<tr>
<td>Underflow</td>
</tr>
<tr>
<td>Overflow</td>
</tr>
</tbody>
</table>

Absolute Pixel Gain (mV/fC)
Chip 6: Distribution of Pixel Offsets

- **Entries**: 45
- **Mean**: 1110 mV
- **RMS**: 11.63 mV
- **Underflow**: 0
- **Overflow**: 0

**Offset (mV)**: 1040, 1060, ..., 1180

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ENC Vs Q at 50V, Chip6.

ENC is under 180\,e^−
ENC is under $180e^-$
Extended Range T1

T1 as a function of Q over extended range.

- $T_{\text{inj}} = 2.5$ ns
- $T_{\text{inj}} = 3.5$ ns
- $T_{\text{inj}} = 4.5$ ns
- $T_{\text{inj}} = 5.5$ ns
- $T_{\text{inj}} = 6.5$ ns

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Extended Range T1 Jitter

T1 Jitter as a function of Q over extended range.

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Extended Range T2

T2 as a function of Q over extended range.

- Tinj = 2.5 ns
- Tinj = 3.5 ns
- Tinj = 4.5 ns
- Tinj = 5.5 ns
- Tinj = 6.5 ns

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Extended Range T2 Jitter

T2 Jitter as a function of Q over extended range.

- Tinj = 2.5 ns
- Tinj = 3.5 ns
- Tinj = 4.5 ns
- Tinj = 5.5 ns
- Tinj = 6.5 ns
Extended Range TOT

TOT as a function of Q over extended range.

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Extended Range TOT Jitter

TOT Jitter as a function of Q over extended range.

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